UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,574	05/21/2007	Dennis May	042933/388814	1966

10949 7590 04/13/2011

Nokia Corporation and Alston & Bird LLP
c/o Alston & Bird LLP
Bank of America Plaza, 101 South Tryon Street
Suite 4000
Charlotte, NC 28280-4000

EXAMINER	
LEE, ADAM	

ART UNIT	PAPER NUMBER
2196	

MAIL DATE	DELIVERY MODE
04/13/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/599,574	MAY, DENNIS	
	Examiner	Art Unit	
	ADAM LEE	2196	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2011* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/03/2011*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 are pending in this application.

Claim Objections

2. As per claim 11, ll. 2, "a mutex" should be "the mutex".

3. As per claim 28, it has similar deficiencies as claim 11.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5, 17-18 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Yue et al. (US 6,272,517) (hereinafter Yue).

5. As per claim 1, Yue teaches an apparatus comprising a processor and memory storing computer program code, wherein the memory and stored computer code are configured, with the processor, to cause the apparatus to at least:

implement a scheduler incorporating an algorithm for ordering the running of threads of execution having different priorities (col. 1, ll. 47-51 describe assigning each thread a priority and put on a run queue), the scheduler maintaining a ready list of threads which are scheduled to

run on the device, ordered by priority (col. 1, ll. 51-59 executing threads by priority); and

implement at least one locking mechanism configured to block access to a resource from all threads except for a thread that holds the locking mechanism (col. 1, ll. 60-67 to col. 2, ll. 1-14 describe blocking threads and sleeping threads while waiting to use the processor),

wherein in an instance in which the scheduler selects a thread on the ready list to run, but the selected thread is blocked from running because a resource it requires is blocked (col. 2, ll. 23-27 describe Thread B being blocked to wait for the lock), the scheduler does not switch to the blocked thread but retains the blocked thread in its place by priority on the ready list (col. 2, ll. 54-64 describe that no context switch is required and col. 9, ll. 5-7 and 14-18 describe the owner thread using the remaining time and not context switching which is interpreted to leave all other threads in their current state) and instead yields to the thread which holds the locking mechanism and causes the thread which holds the locking mechanism to run (abstract, ll. 3-10 and col. 10, ll. 28-31 describe the owner thread of the resource executing while blocking a consumer thread).

6. As per claim 5, Yue further teaches an apparatus according to claim 1 wherein a thread contains a pointer to any locking mechanism it is blocked on (col. 7, ll. 47-49 describe a ticket queue pointer).

7. As per claim 17, it has similar limitations as claim 1 and is therefore rejecting using the same rationale.

8. As per claim 18, it has similar limitations as claim 1 and is therefore rejecting using the same rationale.

9. As per claim 22, it has similar limitations as claim 5 and is therefore rejecting using the same rationale.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2-4, 7, 12, 19-21, 24 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yue in view of Zolnowsky (US 5,826,081) (as cited in previous office action).

11. As per claim 2, Yue fails to explicitly teach wherein states are assigned to threads and the list comprises of all threads having a common state.

12. However, Zolnowsky teaches wherein states are assigned to threads and the list comprises of all threads having a common state (col. 6, ll. 61-67 to col. 7, ll. 1-6 describe scheduling threads together with the same processor affinity).

13. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine thread states as taught by Zolnowsky into the apparatus as taught by Yue because it would allow for priority thread execution (see Zolnowsky col. 5, ll. 16-19) and Yue suggests a need to solve this problem (see Yue col. 2, ll. 30-33).

14. As per claim 3, Zolnowsky teaches a blocked thread is not permitted to change its state (col. 6, ll. 61-67 to col. 7, ll. 1-6 describe threads can only run on processors to which it has affinity).

15. As per claim 4, Yue fails to explicitly teach the ready list is subdivided in accordance with the priority of the threads it contains.

16. However, Zolnowsky teaches the ready list is subdivided in accordance with the priority of the threads it contains (fig. 8 and col. 9, ll. 8-15 describe organizing threads based on priority for real time execution).

17. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine thread priority subdivision as taught by Zolnowsky into the apparatus as taught by Yue because it would allow for priority thread execution (see Zolnowsky col. 5, ll. 16-19) and Yue suggests a need to solve this problem (see Yue col. 2, ll. 30-33).

18. As per claim 7, Yue fails to explicitly teach the scheduler at the end of an interrupt service routine which is caused to run.

19. However, Zolnowsky teaches the scheduler at the end of an interrupt service routine which is caused to run (col. 8, ll. 61-64 describe interrupt threads that are given the highest priority).

20. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine interrupt service routines as taught by Zolnowsky into the apparatus as taught by Yue because it would allow for priority thread execution (see Zolnowsky col. 5, ll. 16-19) and Yue suggests a need to solve this problem (see Yue col. 2, ll. 30-33).

21. As per claim 12, Yue fails to explicitly teach the scheduler is included in a kernel of an operating system of the apparatus.

22. However, Zolnowsky teaches the scheduler is included in a kernel of an operating system of the apparatus (col. 5, ll. 26-31 describe a scheduler in an OS kernel).

23. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine interrupt service routines as taught by Zolnowsky into the apparatus as taught by Yue because it would allow for priority thread execution (see Zolnowsky col. 5, ll. 16-19) and Yue suggests a need to solve this problem (see Yue col. 2, ll. 30-33).

24. As per claim 19, it has similar limitations as claim 2 and is therefore rejecting using the same rationale.

25. As per claim 20, it has similar limitations as claim 3 and is therefore rejecting using the same rationale.

26. As per claim 21, it has similar limitations as claim 4 and is therefore rejecting using the same rationale.

27. As per claim 24, it has similar limitations as claim 7 and is therefore rejecting using the same rationale.

28. As per claim 29, it has similar limitations as claim 12 and is therefore rejecting using the same rationale.

29. Claims 6, 8, 23 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yue in view of Hall ("Engineering Excellence: DEC OSF/1 Symmetric Multi-Processing").

30. As per claim 6, Yue fails to explicitly teach a plurality of non-nestable locking mechanisms.

31. However, Hall teaches a plurality of non-nestable locking mechanisms (pg. 5, col. 2, ll. 14-27 *describe a fast mutex which is read to be analogous to Applicant's non*-nestable locking in *view of Applicant's Specification pg. 12, ll.* 29-30 to pg. 13, ll. 1-6).

32. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine non-nestable locking mechanisms as taught by Hall into the apparatus as taught by Yue because it would provide for a system to have little overhead (see Hall pg. 5, col. 2, ll. 14-19) and Yue suggests a need to resolve poor performance execution (see Yue col. 2, ll. 41-43).

33. As per claim 8, Yue fails to explicitly teach the locking mechanism(s) comprise(s) a mutex including a pointer, which is null if the mutex is free or points to the thread holding the mutex, and includes a flag indicating whether or not the mutex is contested.

34. However, Hall teaches the locking mechanism(s) comprise(s) a mutex including a pointer (pg. 6, col. 1, ll. 37-42 describe a mutex pointer), which is null if the mutex is free or points to the thread holding the mutex (pg. 5, col. 1, ll. 47-54 to col. 2, ll. 1-7 describe lock testing to check if the resource is free) and includes a flag indicating whether or not the mutex is contested (pg. 5, col. 1, ll. 24-26 *describe a "set" and "busy" indicators*).

35. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine a mutex as taught by Hall into the apparatus as taught by Yue because it would

provide for a system to have little overhead (see Hall pg. 5, col. 2, ll. 14-19) and Yue suggests a need to resolve poor performance execution (see Yue col. 2, ll. 41-43).

36. As per claim 23, it has similar limitations as claim 6 and is therefore rejecting using the same rationale.

37. As per claim 25, it has similar limitations as claim 8 and is therefore rejecting using the same rationale.

38. Claims 9-11 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yue in view of Hall as applied to claims 8 and 25, and further in view of Zolnowsky.

39. As per claim 9, Yue and Hall fail to explicitly teach the algorithm is configured to delegate memory management to a replaceable memory model configured in dependence upon a configuration of the apparatus.

40. However, Zolnowsky teaches the algorithm is configured to delegate memory management to a replaceable memory model configured in dependence upon a configuration of the apparatus (col. 4, ll. 66-67 to col. 5, ll. 1-15 describe the memory resource allocation process).

41. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine memory management as taught by Zolnowsky into the apparatus as taught by Yue and Hall because it would provide for real-time scheduling (see Zolnowsky col. 3, ll. 51-57) and Yue suggests a need to resolve poor performance execution (see Yue col. 2, ll. 41-43) and Hall suggests a need for a system to have little overhead (see Hall pg. 5, col. 2, ll. 14-19).

42. As per claim 10, Zolnowsky teaches the memory model is configured to run in either pre-emptible or non-preemptible modes (col. 5, ll. 16-25 describe the preemptive scheduling process).

43. As per claim 11, Hall teaches a mutex is configured to protect the module from running in the pre-emptible mode (pg. 2, col. 2, ll. 17-21 describe a non-preemptive kernel).

44. As per claim 26, it has similar limitations as claim 9 and is therefore rejecting using the same rationale.

45. As per claim 27, it has similar limitations as claim 10 and is therefore rejecting using the same rationale.

46. As per claim 28, it has similar limitations as claim 11 and is therefore rejecting using the same rationale.

47. Claims 13-14 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable Yue in view of Zolnowsky as applied to claims 12 and 29, and further in view of Hall.

48. As per claim 13, Yue and Zolnowsky fail to teach the kernel comprises a microkernel or a nanokernel and where the threads are, respectively, microkernel or nanokernel threads.

49. However, Hall teaches the kernel comprises a microkernel or a nanokernel (pg. 2, col. 2, ll. 17-31) and where the threads are, respectively, microkernel or nanokernel threads (pg. 2, col. 2, ll. 17-31).

50. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine kernels and threads as taught by Hall into the apparatus as taught by Yue and Zolnowsky because it would provide for fast execution (see Hall pg. 5, col. 2, ll. 14-19) and Yue suggests a need to resolve poor performance execution (see Yue col. 2, ll. 41-43) and Zolnowsky suggests a need to support real-time execution (see Zolnowsky col. 3, ll. 49-57).

51. As per claim 14, Yue and Zolnowsky fail to explicitly teach call the scheduler each time the kernel is unlocked.

52. However, Hall teaches call the scheduler each time the kernel is unlocked (pg. 5, col. 1, ll. 46-53 describe the spin lock process).

53. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine calling the scheduler as taught by Hall into the apparatus as taught by Yue and Zolnowsky because it would provide for fast execution (see Hall pg. 5, col. 2, ll. 14-19) and Yue suggests a need to resolve poor performance execution (see Yue col. 2, ll. 41-43) and Zolnowsky suggests a need to support real-time execution (see Zolnowsky col. 3, ll. 49-57).

54. As per claim 30, it has similar limitations as claim 13 and is therefore rejecting using the same rationale.

55. As per claim 31, it has similar limitations as claim 14 and is therefore rejecting using the same rationale.

56. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yue in view of Sanches (US 2003/0018510) (as cited in previous office action).

57. As per claim 15, Yue fails to explicitly teach a mobile computing device.

58. However, Sanches teaches a mobile computing device ([0292], ll. 7-25).

59. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine a mobile device as taught by Sanches into the invention as taught by Yue because it

would allow for notifications to be sent in a low-priority background thread (see Sanches [0292], ll. 19-25) and Yue suggests a need for prioritization of threads (col. 1, ll. 47-59).

60. As per claim 16, Sanches teaches a smart phone ([0292], ll. 7-25).

Response to Arguments

61. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adam Lee whose telephone number is (571) 270-3369. The examiner can normally be reached on Mon-Fri 8:30AM to 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emerson Puente can be reached on (571) 272-3652. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Adam Lee/
Examiner
Art Unit 2196

/Emerson C Puente/
Supervisory Patent Examiner, Art Unit 2196